

IN THE UNITED STATES PATENT OFFICE

Applicant: Peter H. Alfke et al.
Assignee: Xilinx, Inc.
Title: "Circuits and Methods for Analyzing Timing
Characteristics of Sequential Logic Elements"
Serial No.: Not Yet Known File Date: March 17, 2004
Examiner: Not Yet Known Art Unit: Not Yet Known
Divisional of
Serial No.: 10/198,801 File Date: 7/19/2002
Docket No.: X-1039-1D US

Mail Stop Patent Application
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INFORMATION DISCLOSURE STATEMENT


Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant(s) bring(s) to the attention of the Examiner the two (2) references listed in the attached Substitute for Form PTO-1449 (Information Disclosure Statement by Applicant).

All of these references were cited in prior related U.S. patent application Serial Number 10/198,801 filed July 19, 2002 to which this application claims priority. Copies of these references have not been supplied herein since they were previously submitted in the parent case.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully Submitted,



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